I CLAIM:

1. An asynchronous FIFO apparatus for a data processing apparatus having a first clock domain and a second clock domain, the first clock domain being asynchronous with respect to the second clock domain, the asynchronous FIFO apparatus being operable to pass data between the first clock domain and the second clock domain and comprising:

a main FIFO memory operable to store said data to be passed between the first clock domain and the second clock domain, the main FIFO memory being accessible from each of the first clock domain and the second clock domain under the control of an access pointer associated with that clock domain, for one of said first and second clock domains the amount of data accessible per clock cycle being variable;

an auxiliary FIFO memory associated with said one of said first and second clock domains and operable to store the access pointer used to access the main FIFO memory from that clock domain, the access pointer being stored at a location of the auxiliary FIFO memory specified by an auxiliary access pointer; and

routing logic operable to pass the auxiliary access pointer to the other of said first and second clock domains to enable that other of the first and second clock domains to retrieve the access pointer stored in the auxiliary FIFO memory.

2. An asynchronous FIFO apparatus as claimed in Claim 1, wherein the routing logic performs a coding on the auxiliary access pointer in order to generate a coded auxiliary access pointer for passing to the other of said first and second clock domains.

3. An asynchronous FIFO apparatus as claimed in Claim 2, wherein the routing logic performs a gray coding operation on the auxiliary access pointer in order to generate a gray coded auxiliary access pointer.

4. An asynchronous FIFO apparatus as claimed in Claim 1, wherein the main FIFO memory is accessible from the first clock domain under the control of a write access pointer in order to write data into the main FIFO memory, and the main FIFO memory is

accessible from the second clock domain under the control of a read access pointer in order to read data from the main FIFO memory.

5. An asynchronous FIFO apparatus as claimed in Claim 4, wherein:

for said first clock domain the amount of data writeable into the main FIFO memory per clock cycle is variable;

the auxiliary FIFO memory is a write pointer FIFO memory operable to store the write access pointer used to access the main FIFO memory from the first clock domain; and

the routing logic is operable to pass the auxiliary access pointer to the second clock domain to enable the second clock domain to retrieve the write access pointer stored in the write pointer FIFO memory;

the asynchronous FIFO apparatus further comprising read logic in the second clock domain and operable in response to the write access pointer to cause the associated data stored in the main FIFO memory to be read.

6. An asynchronous FIFO apparatus as claimed in Claim 4, wherein:

for said second clock domain the amount of data readable from the main FIFO memory per clock cycle is variable;

the auxiliary FIFO memory is a read pointer FIFO memory operable to store the read access pointer used to access the main FIFO memory from the second clock domain; and

the routing logic is operable to pass the auxiliary access pointer to the first clock domain to enable the first clock domain to retrieve the read access pointer stored in the read pointer FIFO memory;

the asynchronous FIFO apparatus further comprising write control logic in the first clock domain and operable in response to the read access pointer to determine whether the main FIFO memory is full.

7. An asynchronous FIFO apparatus as claimed in Claim 4, wherein:

for both of said first and second clock domains the amount of data accessible per clock cycle is variable, the auxiliary FIFO memory comprising first and second auxiliary FIFO memories, each with associated routing logic;

the first auxiliary FIFO memory being a write pointer FIFO memory operable to store the write access pointer used to access the main FIFO memory from the first clock domain, and its associated routing logic being operable to pass the auxiliary access pointer of the write pointer FIFO memory to the second clock domain to enable the second clock domain to retrieve the write access pointer stored in the write pointer FIFO memory;

the asynchronous FIFO apparatus further comprising read logic in the second clock domain and operable in response to the write access pointer to cause the associated data stored in the main FIFO memory to be read;

the second auxiliary FIFO memory being a read pointer FIFO memory operable to store the read access pointer used to access the main FIFO memory from the second clock domain, and its associated routing logic being operable to pass the auxiliary access pointer of the read pointer FIFO memory to the first clock domain to enable the first clock domain to retrieve the read access pointer stored in the read pointer FIFO memory;

the asynchronous FIFO apparatus further comprising write control logic in the first clock domain and operable in response to the read access pointer to determine whether the main FIFO memory is full.

8. A data processing apparatus comprising:

a first element operating in a first clock domain;

a second element operating in a second clock domain; and

an asynchronous FIFO apparatus as claimed in Claim 1, operable to pass data between the first element and the second element.

9. A data processing apparatus as claimed in Claim 8, further comprising:

a trace module operable to produce trace data indicative of the activity of the first element, the trace module including said asynchronous FIFO apparatus;

wherein the main FIFO memory is accessible from the first clock domain under the control of a write access pointer in order to write into the main FIFO memory the trace data, and the main FIFO memory is accessible from the second clock domain under the control of a read access pointer in order to read from the main FIFO memory the trace data for passing to the second element.

10. A data processing apparatus as claimed in Claim 9, wherein a power supply voltage to the first element is variable, and a clock frequency of the first clock domain is operable to change in dependence on the power supply voltage.

11. A method of passing data between a first clock domain and a second clock domain of a data processing apparatus, the first clock domain being asynchronous with respect to the second clock domain, the method comprising the steps of:

(a) storing within a main FIFO memory said data to be passed between the first clock domain and the second clock domain, the main FIFO memory being accessible from each of the first clock domain and the second clock domain under the control of an access pointer associated with that clock domain, for one of said first and second clock domains the amount of data accessible per clock cycle being variable;

(b) storing within an auxiliary FIFO memory associated with said one of said first and second clock domains the access pointer used to access the main FIFO memory from that clock domain, the access pointer being stored at a location of the auxiliary FIFO memory specified by an auxiliary access pointer;

(c) passing the auxiliary access pointer to the other of said first and second clock domains; and

(d) retrieving, at the other of the first and second clock domains, the access pointer stored in the auxiliary FIFO memory.

12. A method as claimed in Claim 11, further comprising the step, prior to said step (c) of performing a coding on the auxiliary access pointer in order to generate a coded auxiliary access pointer for passing at said step (c) to the other of said first and second clock domains.

13. A method as claimed in Claim 12, wherein said step of performing a coding comprises the step of performing a gray coding operation on the auxiliary access pointer in order to generate a gray coded auxiliary access pointer.

14. A method as claimed in Claim 11, wherein the main FIFO memory is accessible from the first clock domain under the control of a write access pointer in order to write data into the main FIFO memory, and the main FIFO memory is accessible from the second clock domain under the control of a read access pointer in order to read data from the main FIFO memory.

15. A method as claimed in Claim 14, wherein:

for said first clock domain the amount of data writeable into the main FIFO memory per clock cycle is variable;

the auxiliary FIFO memory is a write pointer FIFO memory operable to store at said step (b) the write access pointer used to access the main FIFO memory from the first clock domain;

said step (c) comprises the step of passing the auxiliary access pointer to the second clock domain;

said step (d) comprises the step of retrieving, at the second clock domain, the write access pointer stored in the write pointer FIFO memory; and

the method further comprises the step, in the second clock domain, of reading from the main FIFO memory, in response to the write access pointer, the associated data stored in the main FIFO memory.

16. A method as claimed in Claim 14, wherein:

for said second clock domain the amount of data readable from the main FIFO memory per clock cycle is variable;

the auxiliary FIFO memory is a read pointer FIFO memory operable to store at said step (b) the read access pointer used to access the main FIFO memory from the second clock domain;

said step (c) comprises the step of passing the auxiliary access pointer to the first clock domain;

said step (d) comprises the step of retrieving, at the first clock domain, the read access pointer stored in the read pointer FIFO memory; and

the method further comprises the step, in the first clock domain, of determining, in response to the read access pointer, whether the main FIFO memory is full.

17. A method as claimed in Claim 14, wherein:

for both of said first and second clock domains the amount of data accessible per clock cycle is variable, the auxiliary FIFO memory comprising first and second auxiliary FIFO memories, and said steps (b), (c) and (d) being performed for each auxiliary FIFO memory;

the first auxiliary FIFO memory being a write pointer FIFO memory operable to store at said step (b) the write access pointer used to access the main FIFO memory from the first clock domain, said associated step (c) comprising the step of passing the auxiliary access pointer to the second clock domain, and said associated step (d) comprising the step of retrieving, at the second clock domain, the write access pointer stored in the write pointer FIFO memory; and

the method further comprising the step, in the second clock domain, of reading from the main FIFO memory, in response to the write access pointer, the associated data stored in the main FIFO memory;

the second auxiliary FIFO memory being a read pointer FIFO memory operable to store at said step (b) the read access pointer used to access the main FIFO memory from the second clock domain, said associated step (c) comprising the step of passing the auxiliary access pointer to the first clock domain, said associated step (d) comprising the step of retrieving, at the first clock domain, the read access pointer stored in the read pointer FIFO memory; and

the method further comprising the step, in the first clock domain, of determining, in response to the read access pointer, whether the main FIFO memory is full.

18. A method of operating a data processing apparatus, comprising the steps of:

providing a first element operating in a first clock domain;

providing a second element operating in a second clock domain; and

performing a method as claimed in Claim 11 to pass data between the first element and the second element.

19. A method as claimed in Claim 18, further comprising the step of:

employing a trace module to produce trace data indicative of the activity of the first element, the method as claimed in Claim 11 being performed within the trace module;

wherein the main FIFO memory is accessible from the first clock domain under the control of a write access pointer in order to write into the main FIFO memory the trace data, and the main FIFO memory is accessible from the second clock domain under the control of a read access pointer in order to read from the main FIFO memory the trace data for passing to the second element.

20. A method as claimed in Claim 19, further comprising the step of varying a power supply voltage to the first element, a clock frequency of the first clock domain changing in dependence on the power supply voltage.